Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A local area network, comprising:

a) a data bus having a multiple of eight parallel data lines;

b) a clock bus;

c) a plurality of bus ports coupled to said data bus and said clock bus, each bus port including a transceiver coupled to each of said data lines, an input buffer coupled to said transceivers, an output buffer coupled to said transceivers, and a hardware interface coupled to said buffers, wherein at least two bus ports have different hardware interfaces and wherein data is transferred on the data bus in a repeating, variable length frame, said frame being defined by a plurality of clock cycles, at least one of which is reserved for bidding for access to transmit on the data bus, following the bidding cycle, at least one cycle is reserved for transmission of message length, at least one cycle is reserved for transmission of destination address, and at least one cycle is reserved for the port having the destination address to assert a busy signal on the data bus.

2. (Original) A local area network according to claim 1, further comprising a power bus, each of said bus ports being coupled to said power bus and drawing power therefrom.

3. (Original) A local area network according to claim 1, wherein said hardware interfaces are selected from the group consisting of a serial port link, an Ethernet port link, a USB port link, and a FireWire(TM) port link.

4. (Original) A local area network according to claim 1, wherein said input and output buffers are each two kilobyte FIFOs.

5. (Canceled)

6. (Canceled)

7. (Currently Amended) A local area network according to claim 1 [[6]], wherein each of said ports has a unique address defining a unique priority value.

8. (Original) A local area network according to claim 7, wherein following the bidding cycle, access to the bus is granted to the port having the highest priority and the other bidding port addresses are placed in a queue in order of priority.

9. (Original) A local area network according to claim 8, wherein each port maintains a copy of the queue.

10. (Canceled)

11. (Previously Presented) A parallel bus local area network, including a plurality of ports with each port having a unique address assigned thereto defining a unique priority value, wherein at least two ports have different hardware interfaces, comprising:

a) means for generating a repeating, variable length frame;

b) port control means for bidding for access to the bus during at least one predefined clock cycle of the frame; and

c) a bus controller for granting access to the bidding port having the highest priority and placing the other bidding port addresses in a queue.

12. (Original) Apparatus according to claim 11 wherein each port maintains a copy of the queue.

13. (Original) Apparatus according to claim 11 wherein bidding is only permitted when the queue is empty.

14. (Original) Apparatus according to claim 11 wherein at least one cycle of the frame is reserved for transmission of message length, at least one cycle is reserved for transmission of destination address, and at least one cycle is reserved for the port having the destination address to assert a busy signal on the data bus.

15. (Original) Apparatus according to claim 14 further comprising:

d) means for enabling the port having access to the data bus to transmit a message length during the message length cycle of the frame; and

e) means for enabling the port having access to the data bus to transmit a destination address during the destination address cycle of the frame.

16. (Original) Apparatus according to claim 15, further comprising:

f) means for enabling the port having the destination address to assert the busy signal during the busy cycle of the frame; and

g) means for enabling the port attempting to transmit to the busy port to repeat bidding until the message is sent.

17. (Canceled)

18. (Canceled)

19. (Currently Amended) A local area network, comprising:

a) a data bus having a plurality of parallel data lines; and

b) a clock bus having a clock frequency; and

c) a plurality of bus ports coupled to said data bus and said clock bus, wherein each of said bus ports has a configurable hardware interface and wherein data is transferred on the data bus in a repeating, variable length frame, said frame being defined by a plurality of clock cycles, at least one of which is reserved for bidding for access to transmit on the data bus, following the bidding cycle, at least one cycle is reserved for transmission of message length, at least one cycle is reserved for transmission of destination address, and at least one cycle is reserved for the port having the destination address to assert a busy signal on the data bus.

20. (Original) A local area network according to claim 19, wherein said configurable hardware interfaces are selected from the group consisting of a serial port link, an Ethernet port link, a USB port link, and a FireWire (TM) port link.

21-25. (Canceled)